

DETAILED ACTION

Allowable Subject Matter

Claims 9-15 and 20-32 are allowed.

The following is an examiner's statement of reasons for allowance: prior art does not teach nor render obvious a power amplifier module that has, in combination with other limitations, the detection circuit comprises a sense transistor operable to detect a drain- gate voltage of the power supply transistor; the sense transistor conducting current if the power supply transistor enters a FET linear region of operation and if a drain-source voltage of the power supply transistor is below a gate-source voltage minus a threshold voltage of the power supply transistor; neither does it have the control circuit is operable to control the drive signal in response to the current and to control the drive signal to substantially prevent the power supply transistor from entering a FET linear region operating state and to reduce an absolute amplitude of the drive signal in response to the sense transistor conducting the current; nor does it have a gate of the sense transistor is connected to a gate of the power supply transistor and a source of the sense transistor is connected to a drain of the power supply transistor; nor does it have the sense transistor has a threshold voltage similar to the threshold voltage of the power supply transistor; nor does it have the control circuit comprises an output transistor coupled to the sense transistor and to a signal junction in the drive circuit such that if the sense transistor conducts current, the output transistor becomes active and causes a signal level at the signal point to be reduced.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICIA T. NGUYEN whose telephone number is (571)272-1768. The examiner can normally be reached on 6:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PTN

March 25, 2010

/Patricia T Nguyen/

Primary Examiner, Art Unit 2817